

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Francois Le Maut, et al

Serial Number 10/22,900

Filed: November 26, 2003

Title: System and Method for Re-Sequencing
Data Packets on a Per-Flow Bases

Date: May 20, 2010

Customer No. 25299

Group Art Unit 2419

Examiner: Hooman Houshmand

INTERNATIONAL BUSINESS
MACHINES CORPORATION
Intellectual Property Law
Department
D-YXSA B-002/2
P. O. Box 12195
Research Triangle Park, NC
27709

Brief on Appeal

Director of US Patent and Trademark Office

P. O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

Applicants have given Notice of Appeal from a Final Rejection in this application.

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Real Party in Interest

The real party in interest in this appeal is the assignee, International Business Machines Corporation.

Related Appeals and Interferences

There are no related appeals or interferences.

Status of Claims

Claims 1, 11(as dependent on 1), 13, and 16-21 stand finally rejected under 35 USC 103(a) as being unpatentable over Salamat (US20030012200A1) in view of Sasagawa (US20080253379A1). This rejection is appealed. Claims 1, 11, 13, 16, 17, 19, and 20 are objected to.

Claims 2-9, 11(as dependent on claim2), and 22-23 stand finally rejected under 35 USC 103(a) as being unpatentable over Salamat, in view of Sasagawa, and further in view of Bryers(US20030126233A1). This rejection is appealed. These claims are also objected to.

Claim 12 (as dependent on claim1) stands finally rejected under 35 USC 103(a) as being unpatentable over Salamat in view of Sasagawa and further in view of Yen(US20020150097A1). This rejection is appealed. This claim is, also, objected to.

Claim 12 (as dependent on claim2) stands rejected under 33 USC 103(a) as being unpatentable over Salamat, in view of Sasagawa, and further in view of Bryers and Yen. This rejection is appealed. The claim is, also, objected to.

Claim 14 stands finally rejected under 35 USC 103 (a) as being unpatentable over Salamat, in view of Sasagawa, and further in view of Beshai (US20020083195a1). This rejection is appealed. The claim is also objected to.

Claims 24-29 stand finally rejected under 35 USC 103(a) as being unpatentable over Salamat in view of Bryers. This rejection is appealed. Claims 28 and 29 are objected to.

Claim 30 stands rejected under 35 USC 103 (a) as being unpatentable over Salamat in views of Bryers and further in view of Beshai. This rejection is appealed.

Claims 10, 15, and 21 stand objected to as being dependent on rejected base claims, but would be allowed if rewritten in independent form including all of the limitations of the base claims and any intervening claims. These Claims are not appealed.

In summary, Claims 1-9, 11-14, 16-20, and 22-30 stand rejected under 35 USC 103(a) and are appealed.

Claims 10, 15, and 21 are allowable and are not appealed.

Status of Amendments

An amendment after final was submitted subsequent to the final rejection, but it was not entered.

In addition, a proposed amendment was submitted and discussed with the Examiner, but no agreement was reached.

Summary of Claimed Subject Matter

The claimed subject matter provides a system and method that re-sequence, on a per flow basis, packets of data subsequent to the packets being switched through different planes of a parallel packet switch. Due to different transmission characteristics of different planes within the switch, packets of data from the same flow could arrive at the egress adapter in a sequence different from the sequence in which the ingress adapter places the packets at the input of the switch. The claimed subject matter re-sequences the packets associated with each flow so that they are arranged in the same order in which they were inserted by the ingress adapter.

The system according to teachings of an embodiment of the present invention includes a plurality of output registers; with each register assigns to handle packets from one of a plurality of flows. A controller places each received data packet at a temporary storage location within a packet buffer. A pointer identifies the output register that is associated with a particular flow. Packets which are associated with the particular flow are transferred from the packet buffer to the identified output register whereat it is determined if the packet is next in sequence to packets already received in the output register.

In another embodiment according to teachings of the present invention a cross reference index table with entries associated with each flow is established. Selected parameters from received packets are used to search the table. If a match is found the index is used to identify the output register previously assigned to handle a particular flow.

Independent Claim 1 recites: A system (FIG. 2, pages 9-12) for resequencing per flow data packets (290, FIG. 2, page 9, line 7-page 10, line 1) received by at least one egress adapter (260, FIG. 2, page 10, lines 6-9): a plurality of output registers dynamically assigned (page 17, lines 15-26) to store receive data packets from one of a plurality of flows (shown in Fig. 5, output registers 500 and described at page 16, lines 25-page 17, line 5); means (egress controller 271, shown in Fig. 2, described at page 12, lines 20-24) for allocating a temporary location in a packet buffer (465 shown in Fig. 4, described at page 14, lines 5-9); means (510, Fig. 5, described at page 17, lines 15-page 18, lines 1-2) ,using predefined parameters, for pointing to an output register (540, Fig 5,

page 17, line 20) previously assigned to receive data packets from a corresponding flow; means (271-a programmable computer, ASIC, PLA or other circuit arrangements – described at page 12, lines 15-19), coupled to the allocation means and the pointing means for determining if each received data packets is the next in sequence of the corresponding flow, by comparing (640, Fig. 6 and page 20, lines 25-30) the packet sequence number (PSN) of said each received data packet to the last packet sequence number used by the pointed out register.

Claim 2 depends on Claim1 and incorporates recitations and references set forth above in Claim 1. Claim 2 is patentably distinct by disclosing the pointer that points to the output register associated with a particular flow. Claim 2 recites a first Content Address Memory (CAM 510, FIG. 5, page 17, line 20) wherein each entry (512, FIG. 5, page 18, line 21) includes a search field 515 (FIG.5, page 17, line 21) having a source identifier (Source, FIG. 5), a routing index (RI, FIG. 5), and a priority level (PRTY, FIG. 5) and an associated identifier field including a cross reference index (520, FIG. 5, page 17, line 15-20, page 18, lines 27-28) to point to a previously assigned output register among a plurality of output registers (500, FIG. 5, page 16, line 26).

Claim 3 depends on Claim 2 and incorporates the recitations and references set forth therein. Claim 3 is patentably distinct reciting wherein the identifier field further contains an activity identifier (521, FIG. 5, page 18, line 27) to indicate when a previously assigned output register is no longer active, and a packet sequence number (522, FIG. 5, page 18, line 28) equal to the last packet sequence number received for the last corresponding flow.

Claim 4 depends on Claim 2 and incorporates recitations and references set forth therein. Claim 4 is patentably distinct reciting the means for pointing further comprise means (550, FRL, FIG. 5 page 18, line 32) for providing a new output register to each new flow of data packets.

Claim 5, dependent on Claim 2, incorporates recitations and references of Claim 2. Claim 5 is patentably distinct, reciting wherein the first Content Address Memory further comprises means for preventing over filling of said first Content Addressable Memory. The means include time stamp (TS) 523, FIG.5, page 19, lines 15-23; Free Entry List (FEL) 514, FIG. 5, page 18, lines 20-23; egress controller (a computer 271,

FIG.2, page 12, lines 20-24) executing program shown in FIG.8 flow chart, page 19, line 23 and page 25, lines 21-30.

Claim 6, dependent on Claim 2, incorporates the recitations and references of Claim 2 which are incorporated herein by reference. Claim 6 is patentably distinct claiming, in addition to Claim 2, a second Content Address Memory (400, FIG. 4, page 15, line 11), a routing index (420, FIG. 4, page 15, line 22), a priority level (425, FIG.4, page 15, line 22), packet sequence number (430, FIG. 4, page 15, line 23), and an associated identifier field (435, FIG. 4, page 15, line 27) to give a packet buffer identifier (ID, 410, FIG.4, page 15, line 19) that identifies the storage location allocated to each received packets.

Claim 7, dependent on Claim 1, incorporates recitations and references of Claim 1. Claim 7 is patentably distinct, reciting, in addition to Claim 1, wherein each of the output registers (540, FIG. 5, page 17, line 20) further comprises a packet sequence number (501, FIG. 5, page 19, line 25) and a packet buffer identifier (502, FIG. 5, page 19, line 29) for an in-process data packet; a valid bit-latch (505, FIG. 5, page 19, line 26) to set an active/not active status that indicates if the in-process data packet is already output.

Claim 8, dependent on Claim 7, incorporates recitations and references of Claim 7. Claim 8 is patentably distinct, reciting , in addition to Claim 7, wherein the output registers further comprises a counter (503, FIG. 5, page 19, lines 30-31) to maintain a value , for each flow, the number of data packets stored in the packet buffer (465, FIG. 4, page 14, line 8) waiting to be transmitted.

Claim 9, dependent on Claim 8 incorporates the recitations and references of Claim 8. Claim 9 is patentably distinct reciting, in addition to Claim 8, scheduling means (scheduler 280. FIG. 2, page 11, lines 15-25) for selecting one of the in-process data packets to be out put.

Claim 11 depends on Claim 1. Claim 11 incorporates recitations and references, set forth above, relative to Claim 1. Claim 11 is patentably distinct reciting a free buffer list (470, FIG. 4, page 15, line 5) to allocate a free temporary storage location (ID) to each received data packet (460, FIG. 4, page 15, line 5).

Claim 12, as dependent on Claim 1, incorporates the recitations, references of Claim 1, and further claims the data packets comprise unicast and multicast data packets (page 7, first paragraph). This Claim is patentably distinct.

Claim 12, as dependent on Claim 2, incorporates the recitations, references of Claim 2, and further claims the data packets comprise unicast and multicast data packets (page 7, first paragraph). This Claim is patentably distinct.

Claim 13 depends on Claim 1. Claim 13 incorporates recitations and references, set forth above, relative to Claim 1 and incorporated herein by reference. Claim 13 is patentably distinct including the structure of Claim 1 and further reciting including at least on ingress adapter (200, FIG. 2, page 9, line 5) comprising counting means (210, FIG.2, 360 and 385, FIG.3, page 13, line 28 and page 14, line 2) for sequentially numbering data packets of a same flow.

Claim 14, dependent on Claims 1 and 13, incorporates the recitations, references of these Claims, and recites the ingress adapter (200, FIG. 2, page 9, line 5) further comprises means (205, FIG. 2, page 10, lines 6-8 and page 12, line 12) for load balancing the data packets over a plurality of independent switching planes (250, FIG. 2, page 10, line 26). Claim 14 is patentably distinct.

Claim 16, patentably distinct, describes a method of handling packets receive in an egress adapter. The claim recites: A method (shown in Fig. 6 and described at page 20, lines 5-24) for resequencing per flow the data packets received by at least one destination egress adapter (260, Fig. 2, page 10, line 7), allocating (605, Fig. 6, page 20, line 11) a temporary storage location in a packet buffer(465, Fig.4) to each receive data packet (460, Fig. 4, page 14, line 7); extracting (610, Fig. 6, page 20, line 13) predefined parameters from said each received data packets; using the predefined parameters to search (615, Fig. 6, page 20, line 14) a memory (CRI CAM 510, FIG. 5, page 17, line 25) and identifying a cross reference index (520, FIG. 5, page 17, line 16); using the cross reference index associated with each received data packets to point (625, Fig. 6, page 20, line 18) to a respective output register previously assigned to the corresponding flow of each received data packet; comparing (640, Fig. 6 and page 21, lines 3-4) the packet sequence number of each received data packet to a packet sequence number stored in the

respective pointed output register to determine if said each received data packet is the next in sequence.

Claim 17, a method claim, depends on Claim 16 and is patentably distinct. Claim 17 is carried out by Egress controller 271 (FIG. 2, page 12, lines 20-24), a programmable computer, executing the program shown by the flow chart of FIG. 6. Claim 17 incorporates recitations, references of Claim 16, and recites: assigning (660, FIG. 6, page 22, lines 5 through 13) a new output register (540, FIG. 5, page 17, line 20) and a new Cross Reference Index if no associated Cross Reference Index is found (617, FIG. 6, page 22, line 6) for a received data packet; storing (660, FIG. 6, page 22, line 13) in the new output register the packet sequence number of said received data packet.

Claim 18, method claim, depends on Claim 16 and recites checking (A bit set, FIG.6, page 20, lines 13-20; page 21, line 11). Claim 18 is patentably distinct.

Claim 19, method claim, depends on Claim 18 and recites assigning (650, FIG. 6, page 21, line 14) a new output register if the assigned output register is found inactive; comparing (655, FIG. 6, page 21, line 24) the packet sequence number of the received data packet to the last packet sequence number used by the inactive assigned output register; and storing (690, FIG. 6, page 21, line 27) in the new output register the packet sequence number (PSN) of said received data packet if it is the next in sequence, otherwise storing (670, FIG. 6, page 21, line 32) in the new output register the last packet sequence number (PSNh) used by the inactive assigned output register.

Claim 20, a method claim, depends on Claims 16 or 17 and inherits recitations and references of those claims, discussed above and incorporated herein by reference. Claim 20 is patentably distinct and recites the additional step of releasing (692, FIG. 6, page 21, line 28) the unused Cross Reference Index (CRI 520, FIG. 5, page 17, line 16) after a pre determined time interval. It should be noted that the Cross Reference Index is a part or field of each entry in the CRI CAM (510, FIG. 5, page 17, line 18) Therefore, when the entry is released to the FEL (Free Entry List 514, FIG. 5, line 23) the Cross Ref. Index is also released.

Claim 22, a method claim, depends on Claims 16 or 17 and recites writing in a CAM (ID CAM 400, FIG. 4, page 15, line 11) source identifier (415, FIG. 4, page 15, line 21), the priority level (425, FIG. 4, page 15, line 22), and the packet sequence

number (430, FIG. 4, page 15, line 23) of each receive data packets that is not the next in sequence, the write address being identified by the storage location allocated to said each received data packet (635, FIG. 6, page 20, lines 20-page 21, line 2).

Claim 24, an independent method, recites: providing a plurality of registers (500, Fig.5 and page 16, lines 25 through 31) with each register associated with a flow; providing a cross reference table (510, Fig. 5 and page 17, lines 15-26) with each entry associated with a register within said plurality of registers; receiving (600, FIG. 6, page 20, line 7)a packet (460, Fig. 4 and page 14, lines 5-9); searching the cross reference table (615, Fig. 6, and page 20, lines 7-24) with parameters selected from the packet (610, Fig. 6 and page 20, lines 7-24); if a match is found (616, FIG. 6, page 20, lines 15-20) correlating at least one parameter identified in a register (625, FIG.6, page 20, lines 17-24) associated with said matching entry with parameter in the packet to determine sequence of said packet relative to a packet identified in said associated register (640, Fig. 6 and page 20, lines 25-30).

Claim 25, a method claim, depends on Claim 24 and recites if a match is not found (617, FIG. 6, page 22, lines 5-15) making a new entry (660, FIG. 6, page 22, line 13)for said packet in said cross reference table (CRI CAM, FIG.5, page 22, lines 5-7)and associating a register (685, FIG. 6, page 21, lines 19-23) from said plurality of registers with said packet and flow to which the packet belongs.

Claim 26, a method claim depends on Claim 24 and recites if the packet is in sequence (642, FIG. 6 page 21, lines 3-10) with packet identified in said associated register setting a valid bit (690, FIG. 6, page 21, lines 3-10) to post request for service to egress scheduler.

Claim 27, method Claim, depends on Claim 24 and recites if the packet is out of sequence (656, FIG. 6, page 21, lines 30-page 22, line 4) relative to the packet identified within said associated register reset a valid bit (670, FIG. 6, page 21, line 32) indicating no request is posted to egress scheduler (page 22, line 1).

Claim 28 (independent) recites: a computer readable medium encoded with computer readable code (paragraph at page 2 of the amendment filed on September 13, 2009 replacing paragraph at page 12, lines 20-24 of specification), said computer readable code including a first instruction module with instructions to examine a packet

(600, Fig. 6 and page 20, lines 5-13) and extract a set of predefined parameters (610, Fig. 6 and page 20, lines 5-13); a second instruction module with instructions that use the extracted predefined parameters to search an index table (615, Fig. 6 and page 20, lines 5-13, Fig. 5, 510 and page 17, lines 15-25) having a plurality of entries with each entry associated with a different register; a third instruction module having instructions that correlate parameters stored in an associated register (Fig. 6, 630, 632, 640 and 642, page 20, lines 25- page 21, lines 1-10) to determine sequence of said packet to packets identified in said register, if a match is found between the extracted predefined parameter and an entry in said index table (Fig. 6, 616,620, 625 and 632, page 20, lines 7-24).

Claim 29, dependent on Claim 28, recites: The program product of Claim 28 further including a forth instruction module including instructions for adding an entry for said packet if a match is not found (Fig. 6, 617,619, 660 and page 22, lines 5-13).

Claim 30, independent, recites: a plurality of switching planes (Fig. 2, 250, page 10, line 26 and page 20, lines 7-8); a buffer (Fig. 4, 465 and page 14, line 8) for storing packets transported through said switching planes (Fig. 2, 250); a system for ensuring packets are in predefined sequence, said system including a register stack (Fig. 5, 500 and page 16, line 26) wherein each register is associated with a different flow (page 10, lines 6-12) of a multi flow system; a cross reference index table (Fig. 5, 510 and page 17, lines 15-26) having a plurality of entries with each entry associated with a different register in said register stack; a controller (Fig. 2, 271 and page 12, lines 20-24) that selects parameters from a received packet (page 17, lines 15-26) to search the index table (Fig. 5, 510) and determine sequence of said packet relative to a packet identified in a register associated with a match entry.

Grounds of rejection to be reviewed

The arguments traversing each grounds of rejection are labeled with like alphabetical characters A through F.

A. Whether Claims 1, 11 (as dependent on 1), 13, and 16-21 are obvious under 35 USC 103(a) by the teachings of Salamat (US 20030012200A1) in view of Sasagawa (US20080253379A1).

B. Whether Claims 2-9, 11 (as dependent on Claim 2), and 22-23 are obvious under 35 USC 103(a) by the teachings of Salamat (US20030012200A1) in view of Sasagawa (US20080253379A1) and further in view of Bryers (US 20030126233a10).

C. Whether Claim 12 (as dependent on claim 1) is obvious under 35 USC 103(a) by the teachings of Salamat (US20030012200A1), in view of Sasagawa (US20080253379A1) and further in view of Yen (US20020150097A1).

D. Whether Claim 12 (as dependent on claim 2) is obvious under 35USC 103(a) by the teachings of Salamat (US20030012200A1) in view of Sasagawa (US20080253379A1) further in view of Bryers (US 20030012200A1) and further in view of Yen (US20020150097A1).

E. Whether Claim 14 is obvious under 35 USC 103(a) by the teachings of Salamat (US20030012200A1) in view of Sasagawa (US20080253379A1) and further in view of Beshai (US20020083195A1).

F. Whether Claims 24-29 are obvious under 35USC 103(a) by the teachings of Salamat (US20030012200A1) in view of Bryers (US20030012200A1).

G. Whether Claim 30 is obvious under 35 USC103 (a) by the teachings of Salamat (US20030012200A1) in view of Bryers (US20030012200A1) and further in view of Beshai (US20020083195A1).

Argument

A. Rejection of Claims 1, 11, 13, and 16-21

Claims 1, 11 (as dependent on claim 1), 13, and 16-21 are rejected under 35 USC 103(a) as being unpatentable over Salamat (US 20030012200A1) in view of Sasagawa (US20080253379A1).

Claim 1

(A1) Elements Not Found in References

Applicants contend that the following limitations (a, b, and c), set forth below and elements of Claim 1, are not found or suggested in either Salamat or Sasagawa alone and/ or in combination: (a) a plurality of output registers with each register dynamically assigned to store received data packets from one of a plurality of flows; (b) means for allocating a temporary storage location in a packet buffer to each received data packet; and (c) means, using predefined parameters, for pointing to an output register previously assigned to receive data packets from a corresponding flow.

The Examiner's contention that Salamat discloses (a), (b), and (c) appears to be error. In particular, the Examiner relied on excerpts from Salamat paragraphs [0010], [0028], [0037], and [0039] for disclosing element (a) of Claim 1, (see Final Office Action, page 5, first full paragraph. For brevity, only a summary of each paragraph is provided and not the entire text. Salamat, paragraph [0010], discloses use of reduced memory for storing a narrow range of sequence numbers. Salamat, paragraph [0028], states: "The resequencing engine is seen to further includes sequence space in the form of memory 94 which is allocated for storing sequence numbers of data packets received by the egress board 40". Salamat, paragraph [0037], discloses special conditions under which the egress board may want to store a data packet. It should be noted this is not a general teaching of storing data packets. Instead, it teaches storing a packet if certain conditions occur. Salamat, paragraph [0039], states that resequencing engine 82 can perform operations on 64 traffic streams. In addition, it also states "On any given stream the sequence number [emphasis added] for the last packet successfully resequenced is stored" It should be noted that the resequencing engine 82 is only performing operations on the sequence numbers of packets rather than on the entire packet.

None of the paragraphs identified above teaches or suggests a plurality of registers performing the functions set forth in Claim 1. As a consequence, this element of Claim 1 is not found in Salamat and the Examiner's contention that it does appears to be error.

Regarding the element of Claim 1 that reads: "means for allocating a temporary storage location in a packet buffer to each received data packets," the Examiner did not identify where this teaching is disclosed and / or suggested in any of the references. It is the burden of the Examiner to identify with specificity where in the references the teaching that render a claimed element obvious is found or provide concrete reasons for such a conclusion. As a consequence, applicants contend that this element is not suggested or disclosed in either Salamat or Sasagawa alone or in combination. In addition, applicant argue that the silence of the Examiner ought to be construed as an admission that this element of Claim 1 is not taught by the references.

Regarding the element of Claim 1 that reads: "means, using predefined parameters, for pointing to an output register previously assigned to a corresponding flow", reliance is based on Salamat, paragraph [0039], for disclosing this element. In particular, the Examiner is relying on the portion of paragraph [0039] that reads; "it should be understood resequencing engine 82 can perform operations on 64 distinct traffic streams." As argued above, relative to Claim 1 element (b), and incorporated herein by reference this language relates to operations on sequence number only. In addition, applicants argue that this statement is too general, vague, and uncertain to be the basis for supporting the position that this element of Claim 1 is disclosed or suggested in Salamat. Any conclusion suggesting that the excerpt from Salamat, paragraph 39, suggests this element of Claim 1 appears to be pure speculation. It is applicant's contention that the material and/or teachings relied on to obviate a claim or element of a claim should be concrete and not speculative. As a consequence, this element of Claim 1 is not disclosed or suggested by the references.

(A2) Prima Facie Case of Obviousness Has Not been Established

The rejection of Claim 1 is based upon the Examiner's position that elements (a)-(c) listed above and incorporated herein by reference are found in Salamat. However, as

argued above and incorporate herein by reference, this position appears to be based upon erroneous construction of the teachings in Salamat. No reasonable construction of Salamat is likely to conclude that it teaches any one of (a)-(c). In addition, Sasagawa, secondary reference, does not teach or suggest that which is absent in Salamat. As a consequence, the combination of Salamat and Sasagawa do not teach claim 1 as a whole. It is the burden of the Examiner to establish a prima facie case. The legal precedent and arguments as applied to Claim 18 below are equally applicable and incorporated herein by reference. Therefore, a prima facie case has not been established and Claim 1 is not obvious in view of Salamat and Sasagawa, singly and /or in combination.

(A3) Salamat seems to Teach Away from Claim 1

Claim 1, in part, recites: a plurality of output registers with each register dynamically assigned to store received data packets from a plurality of flows. Applicant's specification teaches that a switch of this type has to support tenths and even hundredths of thousand of flows at any instance (applicants' specification, page 16, lines 18-20). To meet this demand an array of output registers 500 are implemented to handle all that can be supported simultaneously in the egress adapter (page 16, lines 25-28). Because of the large number of flows that have to be handled in the egress adapter, it follows that the array of output registers occupies a relative large memory space in the egress adapter. In contrast, Salamat teaches the use of a small or limited sequence space in the form of memory 94 for storing selected bits of sequence numbers. This teaching of minimum memory space is permeated throughout the Salamat publication (see for example, paragraphs [0002] efficient method of resequencing out of order data packets to minimize router complexity and memory space requirement ; [0010] the memory space required to store a sequence and compare it against incoming data packets is drastically reduced; [0014] With the invention the receipt of packets previously declared loss is handled efficiently with less sequence space requirement; and [0052] advantages.....the ability to provide efficient and confident resequencing of data packets when memory is limited.

It is the contention of applicants that with respect to the memory size the teachings in Salamat are inapposite to that in Claim 1. Therefore, in this regard an artisan viewing the teachings of Salamat, without hindsight of applicants Claim1, would be led

away from using multiple register that suggest a large storage space. The teach away is further evidence that a prima facie case on obviousness has not been established

(A4) Combination Not Supported by Logical/Concrete reasons.

In rejecting Claim 1, the Examiner admits that Salamat does not teach egress adapter (Final Office Action, page 6, line 3). Reliance is based upon Sasagawa for teaching this feature of Claim 1. The rationale for the combination is stated as follows: "It would have been obvious to a person having ordinary skill in the art, to combine the teachings of Sasagawa with Salamat, thus modifying Salamat to include an egress adapter, to specify a variety of routes provided by MPLS."

Applicants respectfully traverse and argue that this rationale is insufficient to support the combination of two references to render Claim 1 obvious. The Manual of Patent Examining Procedure (MPEP) states: "the key to supporting any rejection under 35 USC 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious" (Section 2142). The US Supreme Court in *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385, 1396 (2007) noted that the analysis supporting a rejection under 35 USC 103 should be made explicit. The Federal Circuit has stated, to wit: "rejection on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rationale underpinning to support the legal conclusion of obviousness". In *re Khan*, 441 Fed3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006). This language was approved by the US Supreme Court in *KSR* (op. cit.) at 1396. Finally, there must be some objective reasons to combine the teachings of the references in order to establish a prima facie case of obviousness. Ex parte Levengood, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993).

It is applicants' contention that the rationale set forth above does not appear to meet the standard set forth by the Patent Office, the Board of Patent Appeal and Interference, and the Courts. The rationale appears to be conclusive without supporting reasons. The only part of the rationale that could be characterized as supporting reason is the phrase, to wit: "to specify a variety of routes provided by MPLS". However, this language does not suggest or remotely explain any reasons for the combination. As a consequence, a prima facie case of obviousness has not been established.

(A5) Indicia of Unobviousness

Even if it is determined that a prima facie case of obviousness has been established (a proposition to which applicants disagree), it is applicants' contention that Claim 1 is still patentable over Salamat and Sasagawa alone or in combination. All or at least one of the three elements (a, b, and c) set forth above is not found in Salamat or Sasagawa. The arguments set forth above to support applicants' position that these elements of Claim 1 are not found in the references are incorporated herein by reference. Since at least one of these elements is novel, the system set forth in Claim 1 is also novel. Applicants' specification, page 9, line 22 through page 10, set forth the inability of the prior art to handle unicast and multicast packets in a simple way. One of the objects of the invention is to provide a system that handles both. (Applicants' specification page 7, lines 1-3). By resequencing on a per flow basis, as practiced in Claim 1, both unicast and multicast are handled transparently by the same system. (Applicants' specification, page 27, lines 27-30). As a consequence, the invention provides solutions to a problem and benefits. The novel structure, problem solution and benefits are indicia of unobviousness. It should also be noted that the benefits and problem solved need not be incorporated in the Claim.

Claims 11(as dependent on 1) and 13

Claims 11 and 13 depend on Claim 1. As argued above and incorporated herein by reference, Claim 1 is nonobvious over Salamat in view of Sasagawa. As a consequence, Claims 11 and 13 are, also, nonobvious. *In re Fine*, 837 F. 2d 1071, 5 USPQ 2d 1596 (Fed. Cir. 1980).

Claim 11

Claim 11 is patentably distinct. The free buffer list provides a listing of memory locations whereat packets can be temporarily stored. The buffer list is a novel structure that allows handling of a relatively large number of packets at a relatively high speed. The novel structure and benefits are indicia of nonobviousness.

The Examiner relied on Salamat paragraph [0012] for teaching the invention of Claim 11. Applicants respectfully disagree and traverse. Salamat paragraph [0012] teaches the method used to resequence a packet that has been previously declared lost or

discards. The method measures the distance between the sequence number of the last received insequence packet and the sequence number of the received out of sequence packet and discard or resequence the received packet based upon a predetermined threshold level of distance. The paragraph further states: "the threshold level of distance being a function of the amount of memory in the system that is available for resequencing data packets".

It is applicants' contention that this paragraph including the quoted phrase would not suggest the use of a free buffer list to assign temporary memory allocation to packets as recited in Claim 11. As a consequence this paragraph of Salamat discloses a different invention that that which is recited in Claim 11. Therefore, Claim 11 is patentable over the art of record.

Claim 13

Claim 13 depends on Claim 1 and is patentably distinct. Claim 13 incorporates the recitations and references of Claim 1 which are discussed above and incorporated herein by reference. Claim 13 recites, in part, "at least one ingress adapter comprising counting means (210, 360, and 385) for sequentially numbering data packets of a same flow".

The Examiner admits (applicants agree) that Salamat does not teach ingress adapter (Final Office Action, middle of page 7). The Examiner relied on Sasagawa paragraph [0014] for disclosing ingress adapter and relied upon the combination of Salamat and Sasagawa for rejecting Claim13 on the grounds of obviousness. The Examiner gave the following reason for the combination: "It would have been obvious to a person having ordinary skill in the art, at the time that the invention was made, to combine the teachings of Sasagawa with Salamat, thus modifying Salamat to include an ingress adapter, to specify a variety of routes provided by MPLS".

Applicants respectfully disagree and traverse. The essence of applicants' contention is that the reason to support the rejection appears to be superficial and not in compliance with standard set forth by the Patent Office, Paten Office Board OF appeals and the Courts. The same reason was given by the Examiner in rejecting Claim 1. Applicants' argument to support our contention that the reason was not sufficient to establish a prima facie case of obviousness is set forth under section (A4) above. That

argument is equally applicable and is incorporated herein by reference. As a consequence, a prim facie case has not been established and Claim 13 is patentable over the art of record.

Claim 16

It is applicants' contention that the following elements (labeled herein (d) and (e)) of Claim 16 are not found in Salamat: (d) using the predefined parameters to search a memory and identifying a cross reference index; (e) using the cross reference index associated with each received data packet to point to a respective output register previously assigned to the corresponding flow of each received data packets.

It is not clear from the Final Office Action which portion of Salamat is relied on to support the rejection. However, the Final Office Action on page 8 refers to Salamat paragraphs [0053 and [0012] in alleging that Salamat teaches (d) and (e). Based upon this association applicants assume that the Examiner is relying on these two paragraphs to support the rejection relative to elements (d) and (e). Salamat paragraph [0053] expresses general statements such as: "The information packets may be switched packets, as in the above example, or the information may be in the form of voice packets" etc. Similarly, paragraph [0012] discussed above relative to Claim 1 and incorporated herein by reference teaches the specifics of the method used by Salamat.

It is applicants' contention that no reasonable construction of Salamat, including paragraphs [0012] and [0093], teaches or suggests elements (d) and (e) of Claim 16. Therefore, it appears the assertion that it does is error. As a consequence, a prima facie case of obviousness has not been established.

In rejecting Claim 16, the Examiner admits that Salamat does not teach egress adapter (Final Office Action, page 8, last line). As was done with Claim 1, the Examiner relied on Sasagawa paragraph [0043] for teaching egress adapter and reject Claim 16 based upon the combination of Salamat and Sasagawa. The rationale for the combination is set forth above in A4 and incorporated herein by reference. Applicants assert that the rationale to support the rejection is insufficient. The arguments set forth above in A4 are equally applicable and are incorporated herein by reference. Therefore, based upon the lack of adequate reasoning, a prima facie case of obviousness has not been established.

Furthermore, applicants argue that Claim 16 is novel because at least one of (d) and (e) is not found in any of the references. The claimed method expedites the speed with which a register that is associated with a flow can be determined. The novel structure and benefits are indicia of nonobviousness

Claims 17-20

Claims 17-20 depend on Claim 16 which is nonobvious, based on the above arguments. Therefore, the dependent Claims 17-20 are also nonobvious. In re Fine (opposite).

Claim 17

Claim 17 is patentably distinct. In addition to Claim 16, Claim 17 calls for assigning a new output register and a new Cross Reference Index if no Cross Reference Index is found for a received data packet; and storing in the new output register the packet sequence number of said received data packet. Claim 17 is patentably distinct because it expands the method of Claim 16 so that the resequencing system can handle packets from new flows. Stated another way, Claim 17 provides dynamic allocation of output registers to handle new packets from new flows (applicants specification, page 17, line 15 through page 17, line 2). It is applicants' contention that the recitation of Claim 17 is not found in Salamat. Therefore, a prima facie case of obviousness has not been established relative to the novel process steps or method set forth in Claim 17.

Furthermore, applicants argue that the novel process steps coupled with the dynamic allocation of registers to accommodate new flows indicate indicia of nonobviousness. As a consequence Claim 17 is patentable over the art of record.

In rejecting Claim 17, the Examiner relied on Salamat. With respect to the step "assigning a new output register and a new Cross Reference Index if no associated Cross Reference Index is found for a received data packet" (Claim 17), it appears that the Examiner fails to identify where in Salamat this teaching is taught or suggested. (see rejection of Claim 17, Final Office Action, page 9). It is the burden of the Examiner to provide support for obviousness rejection. Regarding the step of "storing in the new output register the packet sequence number of said received data packet" (Claim 17), the Examiner's remarks, adjoining this element, states: "[0012] the amount of memory in

the system that is available for re-sequencing data packets)”. Applicants’ contend that this teaching of Salamat would not support the “storing “step of Claim 17. Salamat does not teach output registers as part of the resequencing system; so Salamat cannot meet the terms of Claim 17 if it does not teach output registers. As a consequence, the conclusion that Claim 17 is obvious appears to be error based upon inaccurate facts. Therefore, a prima facie case of obviousness has not been established and Claim 17 is patentable over the art of record.

Claim 18

Claim 18, patentably distinct, depends on Claim 16 and recites further comprising checking if the assigned output register is active.

In rejecting Claim 18, the Examiner states: “[0012] the amount of memory in the system that is available for re-sequencing data packet]”.(See Final Office Action, page 9).

Applicants respectfully disagree and traverse. No where in Salamat paragraph [0012] or in the Examiner’s quote is there any reference or mention to check output register. Claim 18 has to be considered as a whole including Claim 16 on which it depends. When considered as a whole, the claimed process covers the method for handling the registers. There are no registers or valid bit associated with Salamat. As a consequence, there is no reason to perform the checking recited in Claim 18. Therefore, the conclusion, based upon inaccurate facts, appears to be error.

It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art, or by a reasonable inference to the artisan contained in such teachings or suggestions. See In re Sernacker, 702 Fed. 2d 989, 995; 217 USPQ 1, 6 (Fed. Cir. 9183) The reviewing courts for the Patent Office requires proof by evidence in order to establish a prima facie case when the proposition at issue is not supported by a teaching in a prior art reference, common knowledge or capable of unquestionable demonstration. See In re Knapp-Monarch Co., 298 Fed. 2d 230, 232; 132 USPQ 6, 8 (CCPA 1961) and In re Cofer, 354 Fed. 2d 664, 668; 148 USPQ 268, 271-272 (CCPA 1966). See also Section 2143 et. seq of the MPEP.

Claim 19

Claim 19, dependent on Claim 18, recites additional actions to be taken if the assigned output register is inactive. Claim 19 is patentably distinct.

In rejecting Claim 19, the Examiner relied upon Salamat paragraph [0012]. (See Final Office Action, pages 9-10).

Applicants respectfully disagree and traverse. Claim 19 has to be considered as a whole in evaluating its obviousness relative to the prior art. Therefore, the condition “if the assigned output register is found inactive” has to be met. However, Salamat does not teach the use of registers; so the condition recited in Claim 19 cannot be met. The arguments and legal precedent as applied to Claim 18 above are equally applicable and incorporated herein by reference.

Claim 20.

Claim 20, dependent on Claims 16 and 17, recites the additional step of releasing the Cross Reference Index after a predetermined time interval. As shown in FIG. 5, each Cross Reference Index is part of an entry in the CRI CAM. As a consequence, releasing the output register releases the Cross Reference Index and visa verse. In addition, each Cross Reference Index is associated with a corresponding flow. Therefore, by releasing a Cross Reference Index when a related flow has no more packets in the output buffer a smaller number of Cross Reference Index can be used to handle a much larger number of flows (page 26, lines 10 through 22. This is a benefit provided by Claim 20. In addition, applicants contend that Salamat does not suggest, disclose or teach the step of Claim 20. Salamat does not use Cross Reference Index in practicing his invention. Therefore, Salamat cannot release that which it does not use. Since Salamat does not suggest this step a prima facie case of obviousness has not been established. Furthermore, applicants argue that the step of releasing the Cross Reference Index is novel coupled with the benefit of reuse is indicia of nonobviousness. Therefore Claim 20 is patentable over the art of record.

In rejecting Claim 20 the following excerpts from Salamat was reproduced at page 10, second to last full paragraph, Final Office Action: “[0053] data packet sequence number validation may be performed at regular intervals), ([0012] re-sequencing engine discard or re-sequences the received data packets based on a predetermined threshold

level of distance, the threshold level of distance being a function of the amount of memory in the system that is available for re-sequencing data packets.

Applicants contend that none of the excerpts mention release much less releasing Cross Reference Index.. Stated another way, the excerpts are silent in providing teachings that would render Claim 20 obvious to one of ordinary skill in the relevant art. In addition, no explanation was given as to why the teachings of the cited excerpts would render Claim 20 obvious. Therefore, it seems the conclusion that the excerpts would suggest Claim 20 to one of ordinary skill appears to be error. Because the conclusion appears to be based on flawed construction of Salamat, a prima facie case has not been established and Claim 20 is patentable over the art of record.

Claim 21

On page 21, Final Office Action, an attempt was made to read Salamat on Claim 21, but on page 26 Claim 21 is identified as Allowable Subject Matter, if rewritten in independent form. Pending final disposition of this appeal, applicants will rewrite Claim 21 in independent form. As a consequence Claim 21 is not on appeal and will not be addressed further in this document.

B. Rejection of Claims 2-9, 11(as dependent on claim 2), and 22-23

Claims 2-9 (as dependent on claim 2), and 22-23 are rejected under 35 U. S. C. 103(a) as being unpatentable over Salamat, in view of Sasagawa as applied to claims 1 and 16 above, and further in view of Bryers (US2003012623A1).

Claims 6 (as dependent on claim 1), 7, 8, and 9

Claim 6, 7, 8, and 9 depend on Claim 1. As argued above and incorporated herein by reference Claim 1 is nonobvious over Salamat and Sasagawa alone or in combination. As a consequence, Claims 6, 7, 8, and 9 are also nonobvious. In re Fine (oppo. cited)

Claim 2

Claim 2 depends on Claim 1 and is patentably distinct. Claim 2 incorporates the recitations and references discuss above and incorporated herein by reference. The claim recites a novel pointer which identifies one of a plurality of registers associated with a

flow. The pointer allows quick determination of the register in which a packet is placed, hence accelerating the re sequencing process. In that regard it is patentably distinct..

In rejecting Claim 2, the Examiner admits Salamat does not teach the recitations set forth in Claim 2 for pointing to one of a plurality of output registers; instead, reliance is based upon Bryers for teaching this pointer. The Examiner then concluded that it would be obvious to modify Salamat to include a CAM with specific routing details, to properly provide network services (Final Office Action, page 11).

Applicants respectfully disagree and traverse with the below arguments.

B1. Prima Facie Case Not Established.

It is applicants' contention that Bryers does not teach "an associated identifier field including a Cross Reference Index to point to a previously assigned output register among a plurality of output registers". In reading Bryers on Claim 2, the Examiner did not specify where this element of Claim 2 is found or suggested in Bryers. Whereas the Examiner specified the paragraphs in Bryers that he believes read on other elements of Claim 2, he did not do so for the element listed above in this paragraph. As a consequence this omission could be construed as evidence of this element not present in Bryers.

It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art, or by a reasonable inference to the artisan contained in such teachings or suggestions. See In re Sernacker, 702 Fed. 2d 989, 995; 217 USPQ 1, 6 (Fed. Cir. 9183) The reviewing courts for the Patent Office requires proof by evidence in order to establish a prima facie case when the proposition at issue is not supported by a teaching in a prior art reference , common knowledge or capable of unquestionable demonstration. See In re Knapp-Monarch Co., 298 Fed. 2d 230, 232; 132 USPQ 6, 8 (CCPA 1961) and In re Cofer, 354 Fed. 2d 664, 668; 148 USPQ 268, 271-272 (CCPA 1966). See also Section 2143 et. seq of the MPEP.

B2. Combination not supported by Logical/Concrete reason

The reason given for combining Salamat and Bryers appears to be stated as "to properly provide network services".(See Final Office Action, page 11, last sentence).

It is applicants' contention that this statement is too broad and general to support the basis to combine references to render a claim obvious. If this were allowed to stand, then most, if not all, combination invention would be in jeopardy of being declared obvious. To prevent this undesirable outcome, it is submitted the reason given to support a rejection under 35 U. S. C. 103 meets the standard set forth by the Patent Office, Board of Appeal, and the Courts. The arguments set forth above under A4, as applied to Claim 1 on this issue are equally applicable and are incorporated herein by reference. As a consequence, a prima facie has not been established.

B3. Modification Would Adversely Affect Principle Of Salamat

The reason for supporting the combination, in part, states: "thus modifying Salamat to include a CAM with specific routing details, to properly provide network services".(See Final Office Action, page 11).

Salamat teaches the use of small or limited sequence space in the form of memory 94 for storing selected bits of sequence numbers. This teaching of minimum memory space is permeated throughout the Salamat publication (see for example, paragraphs [0002] efficient method of resequencing out of order data packets to minimize router complexity and memory space requirement ; [0010] the memory space required to store a sequence and compare it against incoming data packets is drastically reduced; [0014] With the invention the receipt of packets previously declared loss is handled efficiently with less sequence space requirement; and [0052] advantages.....the ability to provide efficient and confident resequencing of data packets when memory is limited.

Based upon the above, it is obvious that Salamat invention requires a small memory space. Modifying Salamat with the CAM (a storage device) suggested by the Examiner would have the undesirable result of increasing the memory space which would be antithetical to teachings (small memory size requirement) set forth in Salamat. It is applicants' contention that such a modification would change the principle and /or objectives of Salamat invention. Such change is deemed impermissible. Therefore, a prima facie case has not been established. (See In re Ratti, 270 Fed. 2d 810, 123 USPQ 349 (CCPA 1959).

Finally, applicants argue even if a prima facie case is deemed to be established (a proposition to which applicants disagree), Claim 2 is still patentable over the art of record.. As argued above and incorporated herein by reference Claim 2 teaches a novel pointer. The pointer also provides the benefit of expeditiously identifying the register that is associated with a particular flow and in which a packet from the particular flow is to be deposited. As a consequence, the resequencing process is expedited. The novel structure and benefits are indicia of nonobviousness.

Claims 3-6

Claims 3-6 depends on Claim 2. As argued above and incorporated herein by reference, Claim 2 is nonobvious. Therefore, Claims 3-6 are also nonobvious. (See *In re Fine* (opp. Cited).

Claim 3

Claim 3 depends on Claim 2 and incorporates the recitations and references set forth above and incorporated herein by reference. Claim 3 is patentably distinct and recites, in part, “an activity identifier to indicate when a previously assigned output register is no longer active”.

In rejecting Claim 3, the Examiner admits (applicants agree) that this element of Claim 3 is not found in *Salamat* and relied on Bryers paragraph [0161] for teaching Claim 3.(Final Office Action, page 12). Applicants respectfully disagree and argue Bryers neither teaches nor suggests this element of Claim 3. Bryers paragraph [0161] relates to Quality –of –service (QOS) as it applies to bandwidth allocation and fairness when minimum bandwidth allocation cannot be met. There is no teaching or suggestion of an activity identifier to indicate when a previously assigned output register is no longer active. Therefore, reliance on Bryers for teaching this element appears to be error.

It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art, or by a reasonable inference to the artisan contained in such teachings or suggestions. See *In re Sernacker*, 702 Fed. 2d 989, 995; 217 USPQ 1, 6 (Fed. Cir. 9183) The reviewing courts for the Patent Office requires proof by evidence in order to establish a prima facie case of obviousness when the proposition at issue is not

supported by a teaching in a prior art reference , common knowledge or capable of unquestionable demonstration. See In re Knapp-Monarch Co., 298 Fed. 2d 230, 232; 132 USPQ 6, 8 (CCPA 1961) and In re Cofer, 354 Fed. 2d 664, 668; 148 USPQ 268, 271-272 (CCPA 1966). See also Section 2143 et. seq. of the MPEP

The reason for forming the combination that render Claim 3 obvious is stated as: “thus modifying Salamat to include a CAM with specific routing details to properly provide network services”. It is applicants’ contention that this reason is insufficient to support combining references to render a claim obvious. The arguments, set forth in A4 as applied to Claim 1 above, are equally applicable and incorporated herein by reference. As a consequence, prima facie obviousness has not been established.

Salamat teaches the use of a relatively small memory and distance/threshold method to re sequence late arrival packets that were previously declared lost. The small memory only store portion of the sequence number associated with a last insequence packet. There is no use or mention of registers in Salamat. Therefore, Salamat would require a substantial reconstruction and redesign to meet the terms of Claim 3. Therefore, a prima facie case has not been established. (See In re Ratti oppo. cited).

Claim 4

Claim 4 depends on Claim 2 and incorporates the recitations and references set forth therein and incorporated herein by reference. Claim 4 is patentably distinct and further claiming means (Free Register List (FRL 550) for providing a new output register to each new flow of data packets.

In rejecting Claim 4, the Examiner admits (applicants agree) that Salamat does not teach this element of Claim 4. The Examiner relied on Bryers paragraph [0161] for teaching this element and concludes by stating that it would have been obvious to combine the teachings of Bryer with Salamat , thus modifying Salamat to include a CAM with specific routing details to properly provide network services. (Final Office Action, pages 12 through 13, first paragraph)

Applicant respectfully disagree with the Examiner and assert that Bryer does not teach or suggest means for providing a new output register to each new flow of data packets. Bryer’s paragraph [0161] relates to Quality Of Service (QOS) as apply to

bandwidth allocation and fairness when minimum bandwidth allocation cannot be met. The recitation of Claim 4 is not disclosed or suggested in this paragraph. The phrase “active traffic” is the last two words of paragraph [0161] and is also mentioned in the rejection. (See Final Office Action, page 12, last line). This relationship leads applicants to conclude that the Examiner is relying on “active traffic” as used in paragraph [0161] to meet the terms of Claim 4. Applicants traverse and argue that such a construction would be a misuse of the phrase. Instead, applicants assert that “active traffic” should be construed in the context of the paragraph from which it is extracted. When “active traffic” is interpreted in the context of paragraph [0161] no reasonable construction would lead one to conclude that this phrase would suggest Claim 4 to an artisan. As a consequence, the assertion that Bryer teachings suggest Claim 4 is error.

It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art, or by a reasonable inference to the artisan contained in such teachings or suggestions. See In re Sernacker, 702 Fed. 2d 989, 995; 217 USPQ 1, 6 (Fed. Cir. 9183) The reviewing courts for the Patent Office requires proof by evidence in order to establish a prima facie case of obviousness when the proposition at issue is not supported by a teaching in a prior art reference, common knowledge or capable of unquestionable demonstration. See In re Knapp-Monarch Co., 298 Fed. 2d 230, 232; 132 USPQ 6, 8 (CCPA 1961) and In re Cofer, 354 Fed. 2d 664, 668; 148 USPQ 268, 271-272 (CCPA 1966). See also Section 2143 et. seq. of the MPEP

The reason for forming the combination that render Claim 3 obvious is stated as: “thus modifying Salamat to include a CAM with specific routing details to properly provide network services”. It is applicants’ contention that this reason is insufficient to support combining references to render a claim obvious. The arguments, set forth in A4 as applied to Claim 1 above, are equally applicable and incorporated herein by reference. As a consequence, prima facie obviousness has not been established.

Salamat teaches the use of a relatively small memory and distance/threshold method to re sequence late arrival packets that were previously declared lost. The small memory only stores portion of the sequence number associated with a packet. There is no use or teachings of registers in Salamat. Therefore, there would be no need or reason to

provide a means as recited in Claim 4. As a consequence, Salamat would require a substantial reconstruction and redesign to meet the terms of Claim 4. Therefore, a prima facie case has not been established. (See In re Ratti oppo. cited).

Claim 5

Claim 5 depends on Claim 2, reciting wherein the first Contents Address Memory further comprises means (514, 523, FIG. 5) for preventing over filling of said first Contents Address Memory.

In rejecting Claim 5, the Examiner admits (applicants agree) that Salamat does not teach Claim 5. The Examiner relied on Bryer's paragraph [0550] CAM for teaching this element of Claim 5. The rejection then states that it would have been obvious to a person having ordinary skill in the art to combine the teachings of Bryers and Salamat, thus modifying Salamat to include a CAM with memory management to properly provide network services.

Applicants respectfully disagree and assert that Bryers paragraph [0550] does not teach or suggest means for preventing over filling of said first Contents Address Memory. Bryers paragraph [0550] teaches a multi entry point form by FIFO/CAM capable of receiving data from multiple sources. There is no teaching or suggestion of a means for preventing over filling as recited in Claim 5. The fact that CAM is mentioned in the paragraph is not enough to suggest to a person of ordinary skill in the art to provide the recitation of Claim 5. Any such conclusion is based on pure speculation and should be rejected out of hand. CAM should be interpreted in the context in which it is used. The paragraph is silent as to over filling, and inserting that which is not suggested by the paragraph would be resorting to hindsight construction which should not be permitted. As a consequence, a prima facie case of obviousness has not been established. The supporting arguments set forth above to support the patentability of Claim 4 are equally applicable and are incorporated herein by reference.

Claim 6

Claim 6 depends on Claim 2 and in addition to the recitations of Claim 2, including the first Contents Address Memory (CAM), claims a second Contents Address Memory with each entry structured as recited in Claim 6. As a consequence, Claim 6 calls for two CAMs, each structured and performing the functions recited therein.

In rejecting Claim 6, the Examiner admits (applicants agree) that Salamat does not teach a second Contents Address Memory wherein each entry including a source identifier, a routing index, a priority level of each stored data packet, and an associated identifier field to give a packet buffer identifier that identifies the storage location allocated to each received data packet. The Examiner relied on Bryers for teaching this element of Claim 6 and concluded that it would have been obvious to a person having ordinary skill in the art to combine the teachings of Bryers with Salamat thus modifying Salamat to include a CAM with specific routing details to properly provide network services.

Applicants respectfully disagree and traverse. Applicants contend Bryers does not teach two CAMS, with the first CAM having each entry structured as recited in Claim 2 (Claim 2 is read into Claim 6, due to Claim 6 dependency on Claim 2) and the second CAM having each entry including “an associated identifier field to give a packet buffer identifier that identifies the storage location allocated to each received data packet”. Bryers paragraph [0550] describes Figure 41 which shows a single CAM 3144. There is no teaching or suggestion that would lead an artisan to incorporate a second CAM. It is also noted, the Examiner did not identify what is being relied on in Bryers to teach “an associated identifier field to give a packet buffer identifier that identifies the storage location allocated to each received data packet” Therefore, the assertion that Bryers teaches that which is lacking in Salamat appears to be error.

The Graham v. Deere test for obviousness under 35 USC 103 is the subject matter of Section 2141 of The Manual of Patent Examining Procedure (MPEP). To briefly restate the three inquiries set forth by the court, in order, are to determine the applicable prior art, then determine the difference between that art and the claimed invention, and then determine whether a person of ordinary skill in the applicable art would know to make the modification necessary to arrive at those differences in view of the prior art applied.

As has been stated by the Court of Appeals for the Federal Circuit in considering matters of appeal from the Board of Appeals within the Patent Office obviousness is a question of law (the Court citing *Graham v. Deere*) but this determination occurs in the context of a factual inquiry regarding the scope and contents of the prior art. The factual inquiry examines what a reference would have taught or suggested to one of ordinary skill in the art at the time of the invention. (*Northern Telecom v. Datapoint Corp.*, 908 Fed 2d 931, 15 USPQ 2d 1321). The Court cautioned against focusing on the obviousness of the differences between the claimed invention and the prior art rather than the obviousness of the claimed invention as a whole as 35 USC 103 mandates (citing *Hybritech, Inc. v. Monoclonal Antibodies, Inc.* 802 Fed. 2d 1367, 231 USPQ 81) and against the use of hindsight reconstruction of what is disclosed in a prior art reference (citing *Grain Processing Corp. v. American Maize Product Co.*, 840 F. 2d 902, 5 USPQ 2d 1788). The Court has quoted approvingly from its decision in *In re Fritch*, 972 F. 2d 1260, 23 USPQ 2d 1780, in which it said :

The mere fact that the prior art may [emphasis added] be modified in th manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.

On the later point, the CAFC has said that the Patent Office, in determining the obviousness of a claimed invention that combines known elements, whether there is something in the prior art as a whole to suggest the desirability, and thus the obviousness of making the combination (citing *Lindeman Maschinenfabrik GmbH V. American Hoist and Derrick Co.*, 730 F. 2d 1452, 221 USPQ 481)

It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art, or by a reasonable inference to the artisan contained in such teachings or suggestions. See *In re Sernacker*, 702 Fed. 2d 989, 995; 217 USPQ 1, 6 (Fed. Cir. 9183) The reviewing courts for the Patent Office requires proof by evidence in order to establish a prima facie case of obviousness when the proposition at issue is not supported by a teaching in a prior art reference , common knowledge or capable of unquestionable demonstration. See *In re Knapp-Monarch Co.*, 298 Fed. 2d 230, 232; 132

USPQ 6, 8 (CCPA 1961) and In re Cofer, 354 Fed. 2d 664, 668; 148 USPQ 268, 271-272 (CCPA 1966). See also Section 2143 et. seq. of the MPEP

The reason for forming the combination that is alleged to render Claim 6 obvious is stated as: “thus modifying Salamat to include a CAM with specific routing details to properly provide network services”. (See Final Office Action, page 14, third full paragraph). It is applicants’ contention that this reason is insufficient. The arguments set forth above in A4 as applied to Claim 1 are equally applicable and are incorporated herein by reference.

It is also applicants contention to modify Salamat with two CAMs, structured as recited in Claim 6, and each CAM performing the functions set forth in Claim 6 would require a substantial reconstruction and redesign. Therefore, a prima facie case has not been established. (See In re Ratti oppo. cited).

Claim 7

Claim 7 depends on Claim 1 and recites each output register further comprise (a) a packet sequence number and a packet buffer identifier for an in-process data packet; and (b) a valid bit latch to set an activity /not activity status to indicate if the in-process data packet is already output.

In rejecting Claim 7, the Examiner relied on Salamat paragraph [0010] for teaching (a), admits that Salamat does not teach (b), and relied on Bryers paragraph [0161] for teaching (b). The Examiner then concludes: “it would have been obvious ...to combine the teachings of Salamat with Bryers , thus modifying Salamat to include a CAM with specific traffic control details to properly provides network services”.(See Final Office Action, page 15, second full paragraph).

Applicants respectfully disagree and traverse. It is applicants’ contention that Salamat does not teach or suggest (a). As argued relative to Claim 1 above and incorporated herein by reference Salamat is silent regarding the teachings of registers; so it follows that there would be no reason to teach a specific structure to format the registers as recited in Claim 7. Salamat paragraph [0010] relates to methods of bit storage and comparison against threshold levels of sequence numbers associated with packets already received and successfully sequenced. There is no mention of register. Therefore,

it would be illogical to conclude that there is a teaching or suggestion for formatting each register as recited in Claim 7. Likewise, (b) is not disclosed in Bryers paragraph [0161] which as argued relative to Claim 3 above and incorporated herein by reference relates to Quality Of Service. There is no teaching or suggestion to structure each register as set forth in Claim 7. Reliance seems to be based upon the phrase “active traffic”, appearing as the last two words of Bryers paragraph [0161]. (See Final Office Action, third line). It is applicants’ contention that a phrase should not be construed out of context; instead, it should be construed within the context of the paragraph from which it is extracted. When interpreted within context it is applicants’ contention that it would not suggest to one of ordinary skill the recitation of Claim 7. Moreover “active traffic” is too indefinite and general to suggest Claim 7.

As a consequence, the Examiner has not met his burden of establishing a prima facie case of obviousness. All the arguments and legal precedent set forth above relative to Claim 6 are equally applicable and are incorporated herein by reference.

In addition, to the argument challenging the sufficiency of the reason for the combination of Salamat and Bryers set forth above relative to Claim 6 and incorporated herein by reference’ it is noted that “CAM” is referred to in the reason for modifying Salamat. (See Final Office Action, page 15, second full paragraph. CAM is not one of the elements or device of Claim 7. Therefore, its use in the reason to combine is irrelevant and supports the argument that the reason is too vague to justify the combination of references to render Claim 7 obvious.

Claim 8

Claim 8 depends on Claim 7 and further claims a counter to maintain a value, for each flow, the number of data packets stored in the packet buffer waiting to be transmitted.

The Examiner relied on Salamat for teaching this feature. (See Final Office Action, page 15, last full paragraph).

Applicants respectfully disagree with the Examiner and traverse. Applicants find the argument complex and somewhat difficult to follow. It may well give a complex summary of Salamat but it has no bearing or relevancy to counter performing the function

set forth in Claim 8. The paragraphs from Salamat referred to on page 15 of the Final Office Action are: [0030], [0052], and [0012]. Paragraph [0030] is the only one that mentions “counter, the others make no reference to counter. Paragraph [0030], in part, states: “the egress board 40 initiate threshold counter 96. Threshold counter 96 can be implemented as any time keeping mechanism used by the resequencing engine 82 to maintain time count of a predetermined amount of time in which an expected sequence number associated with an incoming data packet is to be received”. It is clear from this recitation that the counter in Salamat is used for a purpose different from the purpose for which the counter is used in Claim 8. As a consequence Salamat does not teach or suggest Claim 8.

Reliance on Salamat to teach Claim 8 seems to be error and a prima facie case has not been established. The arguments and legal precedent as applied to Claim 6 above are incorporated herein by reference.

Claim 9

Claim 9 depends on Claim 8 and recites, in addition to the elements set forth in Claim 8, a scheduler for selecting one of the in-process data packets to be output.

The Examiner relied on Salamat paragraph [0012] to reject Claim 9. (See Final Office Action, page 16, first full paragraph).

Applicants respectfully disagree and traverse. It is applicants’ contention that Salamat does not disclose a scheduler as recited in Claim 9. Salamat paragraph [0012] discloses action taken by the egress side of the system when it receives an out of sequence data packet. There is no mention of a scheduler much less one that performs the function set forth in Claim 9. The reliance on Salamat [paragraph [0012] teaching, disclosing or suggesting this feature of Claim 9 appears to be error.

The burden is on the Examiner to establish a prima facie case. The arguments set forth above to support the patentability of Claim 4 are equally applicable and incorporated herein by reference.

Claim 11

Claim 11 depends on Claim 1 or 2, incorporates the recitations and references associated with those Claims, and further claims a free buffer list to allocate free temporary storage location (ID) to each received data packets.

The Examiner relied on Salamat paragraph [0012] for teaching this element of Claim 11. (See Final Office Action, page 16, last paragraph).

Applicants respectfully disagree and traverse. Applicants contend Salamat does not disclose a free buffer list as stated in Claim 11. Salamat paragraph [0012] discloses a method taken by the egress side of the system when an out of sequence packet is received. There is no mention of free buffer list in Salamat paragraph [0012]. The comments of the Examiner on page 16, last paragraph of the Final Office Action cannot be reasonably construed to suggest a free buffer list as recited in Claim 11. As a consequence, reliance on Salamat paragraph [0012] to teach Claim 11 appears to be error.

The burden to establish a prima facie case is on the Examiner. The arguments set forth above to support patentability of Claim 4 are equally applicable and incorporated herein by reference. As a consequence, Claim 11 is patentable over the art of record.

Claim 22

Claim 22, method claim, depends on Claim 16 and calls for writing in a CAM source identifier, priority level, and packet sequence number of each received data packet that is not the next in sequence, the write address being identified by the storage location allocated to said each received data packet.

In rejecting Claim 22, the Examiner admits that Salamat, primary reference, does not teach writing in a CAM source identifier and the priority level. The Examiner relied on Bryers for this teaching and states the reason for the combination as follows: "It would have been obviousto combine the teachings of Bryers with Salamat thus modifying Salamat to include a CAM with specific routing details to properly provide network services". (See Final Office Action, page 17).

Applicants respectfully disagree and traverse. One of applicants' arguments traversing this rejection is that the reason set forth in the Final Rejection is insufficient to support combining references. The arguments set forth under A4 as applied to Claim 1 on this issue are equally applicable and incorporated herein by reference. Another argument is that the suggested combination would adversely affect the principle of Salamat. AS

argued under B3 above and incorporated herein by reference, Salamat requires minimal memory space to store selected bits of the in-sequence sequence number that is compared with sequence number of incoming packets to determine if the packet is out of sequence. A CAM is a storage facility and adding one as suggested by the Examiner would increase the storage capacity of Salamat and in that regard would be adverse to the teachings of Salamat.

Finally, applicants argue that Claim 22 should be considered as a whole in assessing its obviousness relative to the prior art. As a consequence, Claim 16 and Claim 17 must be separately read into Claim 22. In either case Salamat, the primary reference, would have to undergo extensive reconstruction and redesign. Such extensive rework is deemed not establishing a prima facie case. It is the burden of the Examiner to establish a prima facie case. Based upon the above arguments, the burden has not been met. Therefore, Claim 22 is patentable over the art of record...

C. Rejection of Claim 12 (as dependent on Claim 1)

Claim 12

Claim 12 (as dependent on Claim 1) is rejected under 35 U. S. C. 103(a) as being unpatentable over Salamat, in view of Sasagawa as applied to Claim 1 above, and further in view of Yen (US20020150097A1).

Claim 12, dependent on Claim 1, incorporates the recitations and references of Claim 1. In addition to Claim 1, Claim 12 is patentably distinct reciting wherein the data packets comprise unicast and multicast data packets.

In rejecting Claim 12, the Examiner admits Salamat does not teach the data packets comprise unicast and multicast data packets. The Examiner relied on Yen for this teaching. The Examiner then concludes: “it would have been obvious....to combine the teachings of Yen with Salamat, thus further modifying Salamat to include unicast and multicast data packets so that teleconferencing, videoconferencing, and connection-oriented communication are enabled”. (See Final Office Action, page 18, section 8).

Applicants respectfully disagree and traverse. The Court of Appeals for the Federal Circuit has cautioned against focusing on the obviousness of the differences

between the claimed invention and the prior art rather than the obviousness of the claimed invention as a whole as 35 U. S. C. 103 requires (citing *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d1367, 231 USPQ 81) and against the use of hindsight reconstruction of what is disclosed in a prior art reference (citing *Grain Processing Corp. v. American Maize Products Co.*, 840 F. 2d 902, 5 USPQ 2d 1788). When Claim 12 is construed as a whole, the limitations (a)-(c) of Claim 1 identified above and incorporated herein by reference would have to be included in Claim 12. As argued above relative to Claim 1 and incorporated herein by reference, these limitations are not found in Salamat. As a consequence, Salamat would require extensive reconstruction and redesign to meet the terms of Claim 12. Such extensive reconstruction and redesign of the prima reference do not establish a prima facie case of obviousness. (See *In re Ratti*, 270 F. 2d 810, 813, 123 USPQ 349, 352 (CCPA 1959).

In addition, applicants contend the reason given for the combination is not sufficient. The reason should be concrete and at least meets the requirement set forth by the Patent Office, the Patent Office Board of Appeal and Interference, and the Courts. The arguments set forth above under A4 is equally applicable and are incorporated herein by reference. As a consequence a prima facie case has not been established.

D. Rejection of Claim 12 (as dependent on Claim 2)

Claim 12.

Claim 12 as dependent on Claim 2 is deemed obvious under 35 UC 103 (a) in view of Salamat, Sasagawa, Bryers, and Yen.

Applicants respectfully disagree and traverse. The arguments and precedence set forth in section C (immediately above) are equally applicable and are incorporated herein by reference. As a consequence , a prima facie case has not been established against Claim 12 (as dependent on Claim 2).

E. Rejection of Claim 14

Claim 14

Claim 14, dependent on Claims 1 and 13, is rejected under 35 USC 103(a) as being unpatentable over Salamat in view of Sasagawa as applied to Claim 1 above, and

further in view of Beshai (US20020083195A1). The Examiner admits that the load balancing function recited in Claim 14 is not found in Salamat and relied on Beshai paragraph [0122] for teaching Claim 14. The Examiner then concludes that it would be obvious to modify Salamat to include load balancing over a plurality of independent switching planes the data packets to keep delays to a minimum. (See Final Office Action, pages 19-20).

Applicants respectfully disagree and traverse. As argued above relative to Claim 12 and incorporated herein by reference in evaluating the obviousness of Claim 14, the focus should be on Claim 14 as a whole and not on the obviousness of the differences between the Claim and the prior art. (See Hybritch, *oppo. cited*). Claim 14 as a whole incorporates the elements of Claims 1 and 13. As argued above relative to Claim 1 and incorporated herein by reference elements (a)-(c) are not found in Salamat and Sasagawa alone or in combination. As a consequence to meet the recitation of Claim 14 the suggested combination of references would require substantial re construction and re design of Salamat (the primary reference). Therefore, a *prima facie* case as not been established. (See *In re Ratti, oppo. cited*).

F. Rejection of Claims 24-29

Claims 24-29 are rejected under 35 USC 103 (a) as being unpatentable over Salamat in views of Bryers.

Claim 24

Claim 24, an independent method Claim, calls for (a) providing a plurality of registers with each register associated with a flow; (b) providing a cross reference table with each entry associated with a register within said plurality of registers. These two elements are not found in Salamat or Bryers alone or in combination.

The Examiner is rejecting Claim 24 argued that Salamat paragraph [0039] teaches (a). The Examiner admits that Salamat does not teach (b) and relied on Bryers paragraph [0550]. The Examiner then concludes it would have been obvious to combine the teachings of Bryers with Salamat, thus modifying Salamat to include a CAM with specific routing details, to properly provide network services.

F1. Applicants respectfully disagree and traverse. Salamat paragraph [0039] states: “resequencing engine 82 can perform operations on, for example, 64 distinct traffic streams.” The Examiner relied on this teaching to argue it discloses element (a) of Claim 24. This sentence does not even mention register much less teaches the association of each register with a particular flow as recited in (a). Applicants contend that this sentence is too general and indefinite to suggest (a) to one of ordinary skill in the art. Therefore, Salamat does not disclose (a). Likewise, Bryers does not disclose (b) because its teaching of a CAM would not suggest a cross reference table with each entry associated with a register within the plurality of registers. In evaluating elements of a claim, the function that a device performs in the claim must also be considered. It would seem that the functions and association of the registers and cross reference table of Claim 24 was not considered in evaluating Claim 24. As a consequence, the conclusion that (a) or (b) is disclosed in Salamat or Bryers appears to be error. The legal arguments and precedent beginning with *Graham v. Deere* as applied to Claim 6 above is equally applicable and is incorporated herein by reference. The burden is on the Examiner to establish a prima facie case which has not been established for Claim 24.

F2. Even if Salamat and Bryers were to be combined the resultant system would not suggest Claim 24 to an artisan because the synergistic relationship between registers and flows and the cross reference table and the registers recited in Claim 24 would not be present in the combination. Salamat (primary reference) would require significant reconstruction and redesign in order to suggest Claim 24. It has been held that a prima facie case has not been established when such extensive reconstruction and redesign of the prior art is required. (See *In re Ratti*, *op. cit.*).

F3. Furthermore, applicants argue that the reason given for combining the references is insufficient. The supporting reason is, in part stated: “It would have been obvious ...to combine the teachings of Bryers with Salamat, thus modifying Salamat to include a CAM with specific routing details, to properly provide network services” It is applicants contention that this reason is too general and non concrete to be the basis to combine references. The arguments and legal precedent set forth above in A4 on this issue is equally applicable and are incorporated herein by reference. As a consequence, a prima facie case has not been established.

F4. Finally, even if it is deemed that a prima facie case has been established (a proposition to which applicants do not agree), applicants assert that Claim 24 is patentable over the art of record. As argued above, Claim 24 incorporates (a) and (b) and is therefore novel. The problem that is solved and the benefits resulting from the use of registers and synergism with flows are discussed at page 15, line 7 through page 16, line 14, applicants' specification. The novel structure coupled with solving problems and providing benefits are indicia of non-obviousness.

Claims 25-27

Claims 25-27 depends on Claim 24 which as argued above is nonobvious. Therefore, Claims 25-27 are also nonobvious. (See *In re Fine*, *op. cit.*).

Claim 25

Claim 25, dependent on Claim 24, is patentably distinct, claiming if a match is not found making a new entry for said packet in said cross reference table and associating a register from said plurality of registers with said packet and flow to which the packet belongs.

In rejecting Claim 25 the Examiner admits that Claim 25 is not disclosed in *Salamat* and relied on *Bryers* paragraph [0550] for this teaching. The Examiner then concludes that it would have been obvious to modify *Salamat* to include a CAM with specific routing details to properly provide network services. (See Final Office Action, page 21)

Applicants respectfully disagree and traverse. The recitation in Claim 25 further limits claim 24 by specifying actions to be taken if a match is not found in the cross reference table. The actions recited in Claim 25 have to be considered in evaluating the Claim for obviousness against the prior art of *Bryers*. The conclusion of the Examiner that *Bryers* teaches Claim 25 appears to be based upon *Bryers* paragraph [0550] reference to a CAM. Arguably, a CAM could be used as a cross reference table. But Claim 25, a method, recites specific association to be established between the new entries, the registers, and the related flow. The associations which are set forth in Claim 25 are not found in *Bryers*. As a consequence, the conclusion that *Bryers* teaches Claim 25 appears

to be error. The arguments and precedence beginning with *Graham v. Deere* as applied to Claim 6 above are equally applicable and are incorporated herein by reference. The Examiner has the burden to establish a prima facie case and has not done so relative to Claim 25. In addition, the arguments set forth under F2-F4 set forth above to support the patentability of Claim 24 are equally applicable and incorporated herein by reference.

Claim 26

Claim 26 depends on Claim 24 and calls for setting a valid bit to post request for service to egress scheduler if the packet is in sequence with packets identified in said associated register. For reasons set forth below, Claim 26 is patentably distinct.

In rejecting Claim 26, the Examiner relied on Salamat paragraph [0012] and in particular the phrase that reads: “system including an ingress side, an egress side, handling data packets received at the egress side”. (See Final Office Action, page 22, first full paragraph).

Applicants respectfully disagree and traverse. The phrase, set forth above, relied on by the Examiner does not remotely suggest setting a valid bit to post request for service to egress scheduler. To conclude that it does would be based upon pure speculation. Likewise, Salamat paragraph [0012] does not disclose any teaching that could be reasonably construed to suggest setting a valid bit as recited in Claim 26. The phrase relied on by the Examiner does not suggest Claim 26 on its face. In addition, the Examiner has not given any reason or explanation why this phrase and/or Salamat paragraph [0012] teaches Claim 26. As a consequence, there is no support for the conclusion that Salamat suggest Claim 26. It is the burden of the Examiner to establish a prima facie case. The reviewing courts for the Patent Office requires proof by evidence in order to establish a prima facie case of obviousness when the proposition at issue is not supported by a teaching in a prior art reference, common knowledge or capable of unquestionable demonstration. See *In re Knapp-Monarch Co.*, 298 Fed. 2d 230, 232; 132 USPQ 6, 8 (CCPA 1961) and *In re Cofer*, 354 Fed. 2d 664, 668; 148 USPQ 268, 271-272 (CCPA 1966).

Claim 27

Claim 27, dependent on Claim 24, calls for resetting a valid bit indicating no request is posed to egress scheduler if the packet is out of sequence relative to the packet identified within said associated register. This Claim is patentably distinct.

In rejecting Claim 27 the Examiner relied on Salamat and states: “([0012] handling data packets received at the egress side. The resequencing engine discards or re-sequences the received data packets)” See Final Office Action, page 22, second full paragraph..

Applicants respectfully disagree and traverse. It is applicants’ contention that neither Salamat teachings nor the Examiner quote suggest Claim 27. As a consequence, the arguments applied to Claim 26 above are equally applicable and incorporated herein by reference.

Claim 28

Claim 28, independent , recites a computer readable medium encoded with computer readable code including a second instruction module that uses extracted predefined parameters to search an index table having a plurality of entries with each entry associated with a different register; (See second element of Claim 28).

a third instruction module having instructions that correlates parameters in said packets with parameters stored in an associated register to determine sequence of said packet to packets identified in said register if a match is found between the extracted predefined parameter and an entry in said index table.(See last element of Claim 28). As will be argued below these two elements of Claim 28 are not found in Salamat and Bryers alone or in combination.

In rejecting Claim 28, except for the index table, the Examiner relied on Salamat. For the teaching of the index table, the Examiner relied on Bryers. The reason for the combination is stated as follows: “It would have been obviousto combine the teachings of Bryers with Salamat, thus modifying Salamat to include a CAM with specific routing details , to properly provide network services. (See Final Office Action, pages 22-23).

Applicants respectfully disagree and traverse. Every word, condition etc. of a claim must be given weight in assessing the obviousness of the claim relative to the prior

art. The second element of Claim 28, set forth above, comprises the condition that each entry of the index table associated with a different register. This feature, part of the second element of Claim 28, is not found in Salamat or Bryers. Hence, the second element (i.e. second instruction module) of Claim 28 set forth above is not found in Salamat or Bryers. Likewise, the condition, of “if a match is found between the predefined parameter and an entry in said index table”, is not found in Salamat or Bryers. Because the third element of Claim 28 comprises this limitation, it too is not found in Salamat or Bryers.

With respect to the second element of Claim 28, the Examiner seems to be relying on Salamat paragraphs [0010], [0028], [0037], and [0039]. (See Final Office Action, page 22, third paragraph). Applicants have reviewed these sections and assert that no reasonable construction would support a conclusion that any one of the paragraphs would suggest the second element of Claim 28. Likewise, reliance is based upon Salamat paragraphs [0039] and [0012] for teaching the third element (third instruction module) of Claim 28. A review of these paragraphs did not find any teachings that would suggest the third instruction module of Claim 28. As a consequence, there is no evidence to support the conclusion that Claim 28 is obvious. Therefore, the conclusion appears to be error.

The Examiner has the burden to establish a prima facie case of obviousness. As a consequence the arguments as applied to Claim 4 under B2 above is equally applicable and incorporated herein by reference.

In addition, Salamat, the primary reference, would require extensive re-construction and re-design. As applied to Claim 4 above and incorporated herein by reference a prima facie case is deemed not established when extensive rework of the prior art is required. (See *In re Ratti*, *oppo. cited*).

Finally, the reason set forth on page 23 (Final Office Action) appears insufficient. The arguments as applied to Claim 1 under A4 above are equally applicable and incorporated herein by reference.

Claim 29

Claim 29, dependent on Claim 28, calls for fourth instruction module including instructions for adding an entry for said packet to the index table if a match is not found. This Claim is patentably distinct.

In rejecting Claim 29, the Examiner admits that Salamat does teach this element of Claim 29 and relied on Bryers for this teaching. The Examiner then states: "It would have been obvious to combine the teachings of Bryers with Salamat, thus modifying Salamat to include a CAM with specific routing details to properly provide network services".

Applicants respectfully disagree and traverse on the grounds that Salamat would require extensive re-construction and re-design. The arguments as applied to Claim 28 above on this point are equally applicable and are incorporated herein by reference. In addition applicants argue that the reason for combining the references appears to be insufficient. The arguments relative to this issue as applied to Claim 28 above are equally applicable and incorporated herein by reference.

G. Rejection of Claim 30

Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Salamat, in view of Bryers and further in view of Beshai.

Claim 30, an apparatus Claim, comprises the following elements:

(a) a system for ensuring packets are in predefined sequence, said system including a register stack wherein each register is associated with a different flow of a multi flow system;

(b) a cross reference index table having a plurality of entries with each entry associated with a different register in said register stack;

(c) a controller that selects parameters from a received packet to search the index table and determine sequence of said packet relative to a packet identified in a register associated with a match entry.

As will be argued herein none of the above is taught or suggested in the references single or in combination.

In rejecting Claim 30, the Examiner relied on Salamat for teaching the above elements (a), (b), and (c).

Applicants respectfully disagree and traverse. In evaluating a claim for obviousness every word, features, interrelation between elements etc. must be considered. When this is done it is clear that neither (a) or (b) or (c) is disclosed in Salamat. With respect to (a), the Examiner states: “([0039] re-sequencing engine performs operation on different streams)” (See Final Office Action, page 24). Applicants contend that register stack and the relation of each of the registers to a flow is not mentioned in Salamat paragraph [0039] or the Examiner’s quote. In addition, this quote is too general and indefinite to be construed as teaching (a). As a consequence it should be rejected out of hand. With respect to (b), the Examiner states: “([0039] distinct traffic streams)” (See Final Office Action, page 24). Applicants contend that “distinct traffic stream is too indefinite to suggest “a cross reference table with a plurality of entries with each entry associated with a register....”, as recited in Claim 30 element (b) set forth above. As a consequence this too should be rejected out of hand. With respect to (c), the Examiner states: “([0012] re-sequencing engine of the system measures the distance between the sequence number associated with the out of sequence data packet and the sequence number of the last packet that was received in sequence . level of distance, amount of memory in the system that is available to sequence data packet”) . (See Final Office Action, page 25). This quote is a partial description of the method that is practiced by Salamat. No reasonable construction could lead an artisan that it suggests (d). In fact, it goes to show that Salamat invention is different from the invention claimed in Claim 30.

It is the burden of the Examiner to establish a prima facie case. The arguments and legal precedent applied to Claim 4, under B2 above, is equally applicable and are incorporated herein by reference.

In rejecting Claim 30, the Examiner admits (1) Salamat does not teach a cross reference index table and relied on Bryers paragraph [0550] for this teaching, (2) Salamat does not teach a plurality of switching planes, a buffer for storing packets transported through said switching planes and relied on Beshai paragraph [0122] for these teachings. With respect to (1), the Examiner concludes “It would have been obvious....to combines the teachings of Bryers with Salamat, thus modifying Salamat to include a CAM with specific routing details, to properly provide network services. With respect to (2), th Examiner concludes “It would have been obviousto combine the teachings of Beshai

with Salamat, thus further modifying Salamat to include a plurality of switching planes, to keep delay to a minimum”. (See Final Office Action, page 25).

Applicants respectfully disagree and traverse. With respect to Bryers paragraph [0550] it does not disclose or suggest a cross reference index table as disclose in the fourth element of Claim 30. Bryers paragraph [0550] does disclose a CAM, but mere teaching of a CAM is not sufficient to suggest element four of Claim 30, reproduce as c above. As argued above all features of element four must be considered in assessing the obviousness of Claim 30 relative to the prior art. Therefore, a cross reference index table having the structure set forth in Claim 30 must be suggested in Bryers to meet the terms of Claim 30. The mere suggestion of CAM in Bryers would not suggest the cross reference table as recited in Claim 30. As a consequence, the Examiner has not met the burden of establishing a prima facie case. The arguments on this issue as applied to Claim 4 are equally applicable and incorporated herein by reference.

In addition, applicants argue combining the references in the manner suggested by the Examiner would have an adverse effect on the principle of Salamat. The suggested combination would require additional storage. In particular, the storage provided by the CAM and the storage provided by the buffer for storing packets transported through said switching planes. These additions would increase the storage capacity of Salamat. However, Salamat teaching is to effectuate its method with minimal storage. Therefore the suggested modification that adds additional storage would distort the stated principle. The arguments, including locations in Salamat patent where teachings of minimal storage are found, applied to Claim 2 under B3 above are equally applicable and incorporated by reference.

Furthermore, applicants argue Salamat, the base reference, would require extensive re-construction and re-design to suggest Claim 30. Such extensive re-work has been held as not establishing a prima facie case of obviousness. (See *In re Ratti*, oppo. cited).

Finally, the reason proffer for forming the combination appears to be insufficient. The arguments on this issue as applied to Claim 1 under A4 above are applicable and incorporated herein by reference.

Conclusion

For the reasons given herein, it is respectfully submitted that the claims on appeal disclose patentable subject matter over the art of record and should be allowed.

Respectfully submitted,

By: /Joscelyn G. Cockburn/

Joscelyn G. Cockburn

Registration No. 27069

(919) 876-7721

Claims appendix

1. A system for resequencing per flow data packets received by at least one destination egress adapter comprising:

a plurality of output registers with each register dynamically assigned to store received data packets from one of a plurality of flows;

means (271) for allocating a temporary storage location in a packet buffer to each received data packets;

means (510,), using predefined parameters, for pointing to an output register (540) previously assigned to receive data packets from a corresponding flow; and

means (271) coupled to the allocation means and to the pointing means for determining if each received data packet is the next in sequence of the corresponding flow, by comparing the packet sequence number (PSN) of said each received data packet to the last packet sequence number (PSNc,PSNh) used by the pointed output register.

2. The system of claim 1 wherein the means for pointing to an output register comprise a first Content Addressable Memory (510) wherein each entry (512) includes a search field (515) having a source identifier, a routing index and a priority level, and an associated identifier field including a Cross Reference Index (520) to point to a previously assigned output register among a plurality of output registers (500).

3. The system of claim 2 wherein the identifier field further contains an activity identifier (521) to indicate when a previously assigned output register is no longer active, and a packet sequence number (522) equal to the last packet sequence number received for the corresponding flow.

4. The system of claim 2 wherein the means for pointing further comprise means (550) for providing a new output register to each new flow of data packets.

5. The system of claim 2 wherein the first Content Addressable Memory further comprises means (514,523) for preventing over filling of said first Content Addressable Memory.

6. The system of claims 1 or 2 further comprising a second Content Addressable Memory (400) wherein each entry including a source identifier (415), a routing index (420), a priority level (425) and the packet sequence number (430) of each stored data packet, and an associated identifier field (435) to give a packet buffer identifier (ID) that identifies the storage location allocated to each received data packet.

7. The system of claim 1 wherein each of the output registers (540) further comprises:

a packet sequence number (501) and a packet buffer identifier (502) for an in-process data packet; and

a valid-bit latch (505) to set an active/not active status that indicates if the in-process data packet is already output.

8. The system of claim 7 wherein the output register further comprises a counter (503) to maintain a value for_i each flow_i the number of data packets stored in the packet buffer waiting to be transmitted.

9. The system of claim 7 further comprising scheduling means (280) coupled to the determination means for selecting one of the in-process data packets to be output.

10. The system of claim 9 wherein the scheduling means is coupled to each of the valid-bit latches to select one valid-bit latch having an active status.

11. The system of claims 1 or 2 wherein the means (265) for allocating comprise a free buffer list (470) to allocate a free temporary storage location (ID) to each received data packet (460).

12. The system of claims 1 or 2 wherein the data packets comprise unicast and multicast data packets.

13. The system of claim 1 further including at least one ingress adapter comprising counting means (210,360,385) for sequentially numbering data packets of a same flow.

14. The system of claim 13 wherein the ingress adapter further comprises means (205) for load balancing the data packets over a plurality of independent switching planes.

15. The system of claim 14 wherein the at least one ingress adapter further comprising means (220) for scheduling the switching of the data packets over the plurality of independent switching planes.

16. A method for resequencing per flow the data packets received by at least one destination egress adapter comprising:

(605) allocating a temporary storage location in a packet buffer to each received data packet;

(610) extracting predefined parameters from said each received data packets;
using the predefined parameters to search a memory and identifying a cross reference index;

using the Cross Reference Index associated with each received data packet to point (625) to a respective output register previously assigned to the corresponding flow of each received data packet; and

comparing (640) the packet sequence number of each received data packet to a packet sequence number stored in the respective pointed output register to determine if said each received data packet is the next in sequence.

17. The method of claim 16 further comprising:

assigning (660) a new output register and a new Cross Reference Index if no associated Cross Reference Index is found (617) for a received data packet; and

storing (690) in the new output register the packet sequence number (PSN) of said received data packet.

18. The method of claim 16 further comprising checking if the assigned output register is active.

19. The method of claim 18 further comprising:

assigning (650) a new output register if the assigned output register is found inactive;

comparing (655) the packet sequence number of the received data packet to the last packet sequence number used by the inactive assigned output register; and

storing (690) in the new output register the packet sequence number (PSN) of said received data packet if it is the next in sequence, otherwise

storing (670) in the new output register the last packet sequence number (PSN_h) used by the inactive assigned output register.

20. The method of claims 16 or 17 further comprising releasing the unused Cross Reference Index after a predetermined time interval.

21. The method of claim 19 wherein the assigned output registers further comprise a packet buffer identifier that identifies the storage location (ID) allocated to each received data packet.

22. The method of claims 16 or 17 further comprising writing in a Content Addressable Memory, the source identifier, the priority level and the packet sequence number of each received data packet that is not the next in sequence, the write address being identified by the storage location allocated to said each received data packet.

23. The system of claims 1 or 16 wherein the predefined parameters include Priority Level (PTY), Routing Index (RI) and Source Identifier.

24. (Original) A method comprising:

providing a plurality of registers with each register associated with a flow:

providing a cross reference table with each entry associated with a register within said plurality of registers;

receiving a packet;

searching the cross reference table with parameters selected from the packet;

if a match is found, correlating at least one parameter identified in a register associated with said matching entry with parameter in the packet to determine sequence of said packet relative to a packet identified in said associated register.

25. The method of claim 24 further including if a match is not found making a new entry for said packet in said cross reference table and associating a register from said plurality of registers with said packet and flow to which the packet belongs.

26. The method of claim 24 further including if the packet is in sequence with packet identified in said associated register setting a valid bit to post request for service to egress scheduler.

27. The method of claim 24 further including if the

packet is out of sequence relative to the packet identified within said associated register reset a valid bit indicating no request is posted to egress scheduler.

28. A program product comprising:

a computer readable medium encoded with computer readable code, said computer readable code including a first instruction module with instructions to examine a packet and extract a set of predefined parameters therefrom;

a second instruction module with instructions that use the extracted predefined parameters to search an index table having a plurality of entries with each entry associated with a different register; and

a third instruction module having instructions that correlate parameters in said packet with parameters stored in an associated register to determine sequence of said packet to packet identified in said register, if a match is found between the extracted predefined parameter and an entry in said index table.

29. The program product of claim 28 further including a fourth instruction module including instructions for adding an entry for said packet to the index table if a match is not found.

30. An apparatus comprising:

- a plurality of switching planes;
- a buffer for storing packets transported through said switching planes;
- a system for ensuring packets are in predefined sequence, said system including a register stack wherein each register is associated with a different flow of a multi flow system;
- a cross reference index table having a plurality of entries with each entry associated with a different register in said register stack; and
- a controller that selects parameters from a received packet to search the index table and determine sequence of said packet relative to a packet identified in a register associated with a match entry.

Evidence appendix

There is no evidence to be presented in this appendix.

Related proceedings appendix

There are no related proceedings.